Natnael Masresha Zerihun

FPGA & Digital Design Engineer
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Profile

Microsystems electrocins engineer (M.Sc.) with hands-on experience in VHDL and FPGA development, from RTL design and FSMs to testbench verification in ModelSim, synthesis in Intel Quartus Prime, and timing analysis with TimeQuest. I also have a strong background in MEMS and sensor systems, including cleanroom microfabrication, multiphysics simulation, and industrial sensor characterization through my M.Sc. thesis at IDEAS. This combination gives me a solid understanding of both sensor hardware and the digital systems around it. My previous professional software experience also brings strong programming, development tooling, and version-control skills.

Education

Aalto University | USN | BME — Finland | Norway | Hungary
Erasmus Mundus Joint M.Sc. in Smart Systems Integrated Solutions (SSIs) — *Aug. 2024 – Aug. 2026*

- Joint master's across three universities: digital design (VHDL/FPGA), MEMS design and microfabrication, measurement & characterization, and system-level integration of smart sensor systems.
- Three-semester design project taken from concept to functional prototype (wildlife acoustic sensor node with FPGA-based acoustic event classification).

Addis Ababa University — Ethiopia
B.Sc. in Electrical and Computer Engineering | *Computer Engineering major* — *Sept. 2015 – Dec. 2020*

FPGA & Digital Design Projects

Frequency-Measurement & Acoustic Event Classification System | *VHDL, ModelSim, Quartus* — SSIs M.Sc.

- Designed the digital back-end of a wildlife acoustic sensor node: a hierarchical RTL system in VHDL integrating a window-based frequency-measurement core, three band-specific frequency-range detectors, and seven-segment display decoders for real-time classification of acoustic events.
- Implemented a two-stage input synchronizer with edge detection to safely sample the asynchronous input signal before window-based edge counting.
- Parameterized the design with VHDL generics (measurement resolution, system clock frequency, per-band activity/gap thresholds), enabling reuse of one frequency-range detector entity across all three detection bands.
- Verified module- and system-level behavior with ModelSim testbenches and waveform analysis; synthesized with Intel Quartus Prime and analyzed timing with TimeQuest.

Parameterized Password-Verification FSM | *VHDL, ModelSim* — SSIs M.Sc.

- Designed a nine-state finite-state machine in VHDL (enumerated state types) that validates a multi-digit input sequence and drives accept/reject indicator outputs.
- Verified correct-sequence and multiple wrong-sequence paths in ModelSim with a generic-mapped testbench.

Synchronous RTL Building Blocks & Testbench Suite | *VHDL, ModelSim* — SSIs M.Sc.

- Implemented a set of synchronous digital modules in VHDL: event counters, shift registers, a Mealy sequence-detector FSM, and BCD counters with seven-segment display decoding.
- Developed a dedicated ModelSim testbench per module with clock/stimulus generation and waveform-based verification, managed as a single ModelSim simulation project.

System-Level Digital Twin of a MEMS Acoustic Sensor Node (Design Lab) | *Twin Builder* — SSIs M.Sc.

- Integrated a piezoelectric MEMS microphone reduced-order model, an analog front-end, and the VHDL detection logic above into one system-level digital twin in Ansys Twin Builder.
- Designed a two-stage amplifier at transistor level in Cadence (topology comparison, hand calculations, simulation) and a VCO behavioral model in VHDL-AMS.

Experience

Thermal Sensor Characterization & Shutterless Calibration (M.Sc. Thesis) Jan. 2026 – June 2026
IDEAS – Integrated Detector Electronics AS *Oslo, Norway*

- Characterized an uncooled LWIR microbolometer FPA (Lynred ATTO640D, 640×480, 12 µm pitch, 8–14 µm band) against a blackbody source over a 0–110 °C sweep; derived per-pixel SiTF, responsivity, and NETD (minimum median NETD ≈99 mK).
- Developed and compared shutterless non-uniformity correction (NUC) methods (one-/two-point, lookup-table library, temperature-indexed interpolation, scene-based) with image-quality metrics for automatic matrix selection at runtime.
- Built the real-time acquisition, streaming, and remote-control platform (Python/FastAPI backend, React web client) used for all measurements and demonstrations.

ML Engineer & Fullstack Developer Jan. 2023 – Sept. 2024
Adludio Ltd *London, UK (remote)*

- Developed a web-based creative design studio and data/ML pipelines for interactive advertising; reduced creative delivery time by ≈85% through reusable design abstractions.

Fullstack Developer | R&D March 2021 – Sept. 2022
CNET Software Technologies *Addis Ababa, Ethiopia*

- Developed APIs, dashboards, and ERP/LMS web applications using .NET Core, Blazor, and Python.

MEMS & Microsystems Projects

Cleanroom Microfabrication of Silicon Microstructures | *Photolithography, Etching, PVD* SSIs M.Sc.

- Executed a full microfabrication flow on Si wafers: thermal oxidation, UV photolithography, ICP dry etching of SiO_2, anisotropic wet etching, and thermal evaporation of Al/Cu bilayers; verified each step with stylus profilometry and ellipsometry.

Piezoelectric MEMS Microphone – Design & FEM Simulation | *COMSOL Multiphysics* SSIs M.Sc.

- Redesigned and simulated a circular-membrane piezoelectric MEMS microphone (coupled solid mechanics/electrostatics); improved sensitivity from 1.1 to 3.21 mV/Pa through material substitution and tuned membrane resonance to the target acoustic band.

MEMS Accelerometer – Coupled Simulation & ROM Generation | *ANSYS, Twin Builder* SSIs M.Sc.

- Performed coupled electrostatic–structural FEM simulation of an electrostatic MEMS accelerometer; validated against analytical hand calculations (1–10% deviation) and generated a reduced-order model for system-level simulation.

Wildlife Acoustic Monitoring Sensor Node (Animal Watch) | *MEMS microphones, Raspberry Pi, ML*SSIs M.Sc.

- Designed a solar-powered elk-monitoring node integrating MEMS/USB microphone arrays on Raspberry Pi with TDOA localization and ML sound classification.

Technical Skills

FPGA & Digital Design: VHDL, synchronous RTL design, FSMs (Mealy/Moore), counters & shift registers, input synchronization & edge detection, parameterized (generic) design, hierarchical/structural design, testbench development
Design Aautomation Tools: ModelSim (simulation, .do wave scripts), Intel Quartus Prime, TimeQuest STA, Cyclone III FPGA, Cadence (analog IC), LTSpice
MEMS & Sensors: Cleanroom microfabrication (photolithography, wet and dry etching, deopsition), COMSOL Multiphysics, ANSYS Workbench & Twin Builder (ROM), sensor calibration & radiometric characterization (NETD/SiTF)
Embedded & Test: LabVIEW (NI DAQ, HIL testing), Raspberry Pi, Arduino
Characterization: WLI/VSI, PSI, profilometry, XRD, XRF,SEM, EDS/EDX, TEM
Programming: Python (NumPy, OpenCV, Matplotlib, FastAPI), C#, JavaScript/TypeScript, Git