Development of Microstructures on Silicon Wafers Using Standard Cleanroom Fabrication Techniques

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***Abstract*—This report presents the fabrication and characterization of three silicon-based wafers using standard microfabrication techniques. The process began with wafer preparation and cleaning, followed by photolithography, dry and wet etching, and metal deposition. Characterization tools such as profilometry and ellipsometry were used to measure layer thicknesses and evaluate process accuracy. Profilometry results indicated consistent photoresist and patterning heights, while ellipsometry measurements were used in comparing the SiO_2 thickness deviations and Transitions. After wafer cleaning with isopropanol and DI water photolithography steps were successfully carried out. Dry etching of SiO_2 using CHF_3/Ar and subsequent O_2 plasma aching effectively defined the intended patterns, while wet etching using KOH demonstrated anisotropic behavior with time-dependent etch depth. Finally, aluminum and copper layers were deposited using thermal evaporation, achieving clean, uniform bilayers. The results from each fabrication step were measured, presented, and discussed in this report. Overall, the lab demonstrated key microfabrication processes and highlighted the importance of precise control at each step to ensure reliable device outcomes.**

***Index Terms*—Microfabrication, Photolithography, etching, sputter deposition**

I. Introduction

Microfabrication is the cornerstone technology in the development of semiconductor devices, enabling the creation of complex, miniaturized components essential to modern electronics such as smartphones, sensors, and biomedical systems [1]. It is built on the precise, highly controlled manipulation of silicon wafers through iterative process steps including patterning, etching, and material deposition.

This report presents a structured microfabrication workflow performed in a cleanroom environment, aimed at replicating key stages of a standard semiconductor process flow. The experimental sequence consisted of five integrated modules: wafer preparation and oxidation, photolithographic patterning, dry plasma etching, wet chemical etching, and thermal metal deposition. At each stage, characterization tools such as stylus profilometry and ellipsometry were used to assess film thickness, etch depth, and surface topography.

Photolithography served as the central patterning step, involving the coating of the wafer with photoresist, exposure to UV light through a photomask, and chemical development to define high-resolution patterns [2]. Etching steps—both dry and wet—were employed to selectively remove material, balancing directionality with selectivity. Finally, copper was deposited using physical vapor deposition (thermal evaporation) to simulate interconnect formation.

The purpose of this report is to synthesize the outcomes of each module into a cohesive narrative that reflects the technical precision and interdependence of microfabrication processes. Emphasis is placed on the theoretical background, procedural execution, and measurement-based analysis required to achieve reliable and repeatable pattern transfer.

II. Fabrication Flow and Tools

This section presents an overview of the primary process steps used in the fabrication flow, including substrate preparation, oxide growth, photolithographic patterning, etching, and metal deposition. Additionally, the characterization tools employed to monitor key parameters such as film thickness and surface topography are described.

A. Process Flow

1) Wafer Preparation and Cleaning: Wafer preparation and cleaning are fundamental steps in microfabrication to ensure the surface is free of contaminants before any processing begins. Fig. 9 shows a (100) Si-wafer. Silicon wafers are commonly cleaned to remove particles, organic residues, and metal ions that may affect the quality and uniformity of subsequent layers. The cleaning process in this lab included rinsing with isopropanol and deionized (DI) water, followed by nitrogen gas drying. These steps are essential to ensure proper adhesion of photoresist during photolithography and to prevent defects in deposited or etched layers. Although not used in this specific step, acetone is also a widely used solvent in wafer cleaning due to its effectiveness in dissolving organic materials.

Fig. 1: Silicon Wafer Substrate Preparation

2) Oxide Growth by Thermal Oxidation: The formation of silicon dioxide (SiO_2) layers on silicon substrates is

a fundamental step in microelectronic and MEMS fabrication. Several deposition and growth techniques are available, each offering distinct advantages in terms of film quality, thermal compatibility, conformality, and process integration. Thermal oxidation is the most established method, producing a dense, uniform oxide by exposing the silicon wafer to high-temperature oxidizing environments (typically 900–1100 °C). Fig. 2 illustrates a wafers structure after oxidation process.The resulting oxide exhibits excellent electrical insulation, mechanical stability, and etch resistance. Other techniques include Plasma-Enhanced Chemical Vapor Deposition (PECVD), which operates at lower temperatures (150-–400 °C) and is often used for structural or protective layers. Low-Pressure CVD (LPCVD) and Atomic Layer Deposition (ALD) offer improved uniformity and thickness control, while PVD methods such as sputtering or e-beam evaporation are also used but less frequently due to limited step coverage and lower film density.

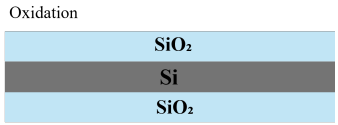
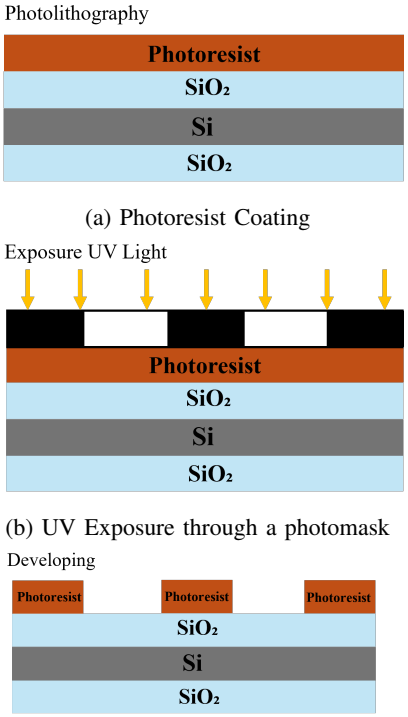


Fig. 2: Thermal Oxidation of Silicon

3) Photolithographic Patterning: Photolithography is a key process used to transfer microscale patterns onto a wafer surface by selectively exposing a light-sensitive material known as photoresist. The process consists of sequential steps including photoresist coating, soft baking, UV exposure, development, and hard baking [3]. A uniform thin film of photoresist is applied to the wafer using spin coating, where a liquid photoresist is dispensed and spread by centrifugal force. The resulting film thickness is controlled by the spin speed, resist viscosity, and spin duration. After coating, a soft bake is performed to remove residual solvents and improve the mechanical and thermal properties of the resist. This step enhances adhesion to the substrate and minimizes internal stress, while also preventing defects such as standing waves and swelling during development [4]. Bake conditions must be optimized carefully—underbaking may leave solvent residues that compromise pattern fidelity, while overbaking can harden the resist and reduce photosensitivity. The baked wafer is then exposed to ultraviolet (UV) light through a photomask, which contains an opaque pattern corresponding to the desired layout. UV exposure induces photochemical reactions in the resist that modify its solubility. In positive-tone resists, the exposed regions become more soluble in the developer; in negative-tone resists, the opposite occurs. For the process used here, a positive-tone resist was employed. After exposure, the wafer is developed using a chemical solution such as tetramethylammonium hydroxide (TMAH), which selectively dissolves the UV-exposed areas of the resist. This results in a patterned resist layer that defines the regions to be etched or modified in subsequent steps. The three main stages of photolithography



(a) Photoresist Coating

(b) UV Exposure through a photomask

(c) Development of PR

Fig. 3: Photolithography stages

is illustrated in Fig. 3. Finally, a hard bake is carried out to stabilize the patterned resist. This baking step improves adhesion, reduces outgassing during vacuum processing, and enhances the resist's durability against subsequent plasma or wet etching. However, care must be taken not to overbake, as it can lead to profile distortion or pattern reflow.

4) Dry Etching: After creating a resist pattern, the pattern transfer process continues with etching the exposed regions of the underlying material. *Etching* is the removal of some portion of the thin film or substrate. The resist serves as a protective layer over areas that should remain intact, while the uncovered sections are subjected to etching. During etching, the exposed material is removed through chemical and/or physical means. Certain materials can undergo spontaneous chemical etching without the need for external agents [1], [5].

There are two main types of etching techniques: *dry etching* and *wet etching*, each with its own advantages and disadvantages.

Dry etching relies on gases and plasma instead of liquid chemicals. Although it is more expensive than wet etching, dry etching offers better process control, higher resolution, and minimizes undercutting.

For the dry etching process, an ICP (Inductively Coupled Plasma) etching system can be used. This system consists of two main chambers: the load lock chamber (Chamber 1) and the process chamber (Handler). Before starting any work, it is essential to ensure the chambers are clean and ready for use. The correct parameters such as RF power, chamber pressure,

etching time, and the type of gases must be properly set.

ICP chambers operate in a vacuum environment. A roughing pump lowers the pressure in the load lock chamber from atmospheric level to around 10^{-2} to 10^{-3} Torr. Only after the pressure drops below 10^{-2} Torr can the wafer be transferred to the process chamber.

The process chamber is maintained at an even lower pressure, typically between 10^{-3} and 10^{-8} Torr, using a high-vacuum pump such as a turbo pump. A schematic diagram of the ICP plasma etching system is shown in Fig. 4, reproduced from [6].

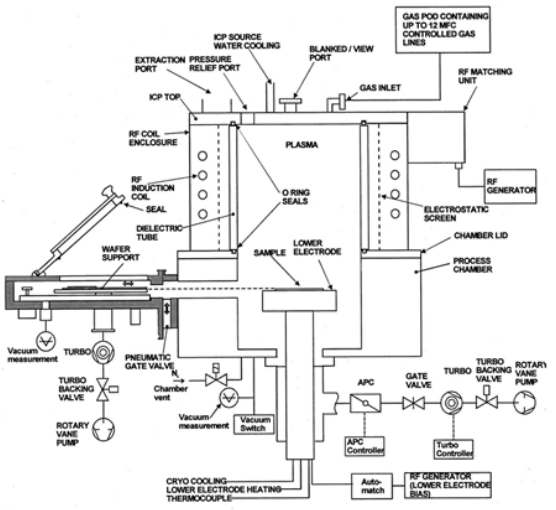


Fig. 4: The design drawing of the ICP plasma etching system. Reproduced from [6]

It is important to understand why a vacuum environment is essential during the etching process. First, it creates a clean environment with minimal contamination. Second, a vacuum is necessary to generate and sustain plasma, as it allows electrons to accelerate and ionize gas molecules effectively. Additionally, the vacuum helps guide ions in a directional path, reducing ion scattering and making the etching process more anisotropic.

Once the vacuum system is stabilized and everything is set, etching gases are introduced. A mixture of gases can be used for an effective etching process. We can use a combination of CHF_3 (trifluoromethane) and Ar (argon). CHF_3 primarily contributes to the chemical etching process by releasing fluorine radicals, which are effective for etching materials like SiO_2 or even Si_3N_4. This makes CHF_3 useful for selective etching.

Argon, on the other hand, is a heavy, inert gas that does not participate in chemical reactions. Instead, it contributes to physical sputtering, which helps enhance anisotropy in the etch profile.

After the dry etching process, the wafer structure should resemble the one shown in Fig. 5 it is time to remove the photoresist (PR) layer. Photoresist can be effectively removed by exposing the wafer to a plasma that selectively targets organic materials like PR. Oxygen plasma (O_2 plasma) is commonly used for this purpose. Since PR is rich in carbon, O_2 plasma—also known as O_2 ashing—can efficiently break it down and remove it without damaging the underlying SiO_2 or Si layers.

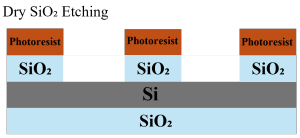


Fig. 5: Dry Etching of SiO_2 Layer

5) Wet Etching: Following dry etching and oxygen plasma removal of the residual photoresist, the next stage in the fabrication process is wet etching. While dry etching provides high directionality and precision due to anisotropic ion bombardment, wet etching offers superior material selectivity and is often employed where uniform layer removal or undercutting is desired. Wet etching uses liquid-phase chemical solutions to remove targeted materials from the wafer surface. Unlike dry etching, which is highly directional, wet etching proceeds isotropically, meaning material is removed equally in all directions. This makes it ideal for bulk thinning or processes where directionality is not critical.

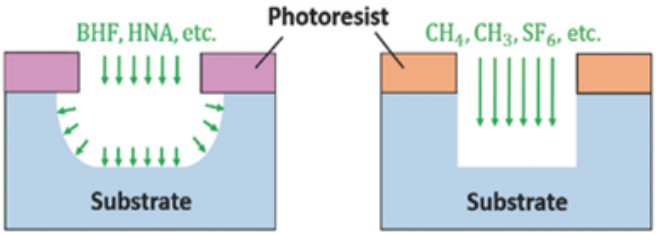


Fig. 6: Schematic comparison between Wet etching (left) and Dry etching (right)

Fig. 6 illustrates the contrast between isotropic wet etching and anisotropic dry etching, Fig. 8 shows how the wafer looks after the deposition steps. Among wet etchants, potassium hydroxide (KOH) is widely used for silicon due to its orientation-dependent etch characteristics. It exhibits a significantly faster etch rate along $\langle 100 \rangle$ direction than $\langle 111 \rangle$ direction, enabling precise formation of V-grooves, cavities, and membranes through natural etch-stop behavior. KOH etching of silicon is an electrochemical process involving both oxidation and dissolution. The overall reaction sequence includes the formation of soluble silicate complexes and the release of hydrogen gas, typically visible as bubbling during etching:

$$\mathrm{Si} + 2\,\mathrm{OH}^- \longrightarrow \mathrm{Si(OH)_2}^{2+} + 4\,\mathrm{e}^-$$

$$4\,\mathrm{H_2O} + 4\,\mathrm{e}^- \longrightarrow 2\,\mathrm{H_2} + 4\,\mathrm{OH}^-$$

$$\mathrm{Si(OH)_2}^{2+} + 4\,\mathrm{OH}^- \longrightarrow \mathrm{SiO_2(OH)_2}^{2-} + 2\,\mathrm{H_2O}$$

$$\mathrm{Si} + 2\,\mathrm{H_2O} + 2\,\mathrm{OH^-} \longrightarrow \mathrm{SiO_2(OH)_2}^{2-} + 2\,\mathrm{H_2}\uparrow$$

The etch rate depends on multiple factors including KOH concentration, temperature, and wafer crystallographic orientation. [7] proposed an empirical model for silicon etching in KOH:

$$R = k_0[\mathrm{H_2O}]^{1/4}[\mathrm{KOH}]^{1/4} \cdot e^{-E_a/kT} \tag{1}$$

Where $E_a = 0.595$ eV and $k_0 = 2480\ \mu\mathrm{m/h} \cdot (\mathrm{mol/L})^{-4.25}$. For example, at 70°C in 10% KOH, the typical etch rate for silicon along $\langle 100 \rangle$ direction is approximately 46 μm/h, which is widely used as a reference in MEMS and IC fabrication. In many fabrication protocols, dry and wet etching are used in combination to leverage their complementary advantages. Dry etching is first used to define sharp, directional features, while wet etching follows for material removal or to achieve lateral etch profiles, particularly after resist stripping. This combined approach enables finer control over geometry, profile shape, and layer selectivity in complex microstructures [8]. Fig. 7 shows wet etching of silicon layer, with SiO_2 serving as a mask.

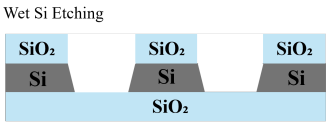


Fig. 7: Wet Etching of Silicon Substrate

6) Metal Deposition: Metal deposition is a critical process in microelectromechanical systems (MEMS) fabrication that involves the controlled application of thin metal films onto substrate materials. These metal layers serve various functions including electrical conductivity paths, electrode formation, reflective surfaces, and structural components. The thickness of these depositions typically ranges from several nanometers to a few micrometers, and require parameter control to achieve the desired film properties including uniformity, adhesion and resistivity. Common metal deposition techniques include physical vapor deposition (PVD) methods such as sputtering and evaporation, and chemical vapor deposition (CVD). Sputtering typically uses Argon bombardment to eject atoms from a target, producing films with good adhesion and uniformity but induces higher residual stresses. Evaporation involves heating the source material to form a vapor that condenses on the substrate, resulting in purer, low-stress films with poorer step coverage. The evaporation rate follows the relationship:

$$N = N_0 \exp\left(-\frac{\Phi_e}{kT}\right) \tag{2}$$

Where N represents the number of atoms evaporating from the surface, N_0 is a material-dependent constant, Φ_e is the activation energy for evaporation, k is Boltzmann's constant, and T is the absolute temperature. This equation (2) demonstrates that the rate of evaporation is directly proportional to the temperature and inversely proportional to the activation energy. Chemical Vapor Deposition (CVD) relies on surface chemical reactions of precursor gases to form highly conformal films, though often at elevated temperatures that may limit substrate compatibility. The choice of deposition method significantly affects MEMS device performance. Advanced methods such as Atomic Layer Deposition (ALD) offer precise and uniform coatings with excellent thickness control [9], making them ideal for nanoscale fabrication.

In metallization schemes, copper is used as a conductor due to its superior electrical conductivity. When implementing copper metallization, aluminum often serves as a partial diffusion barrier and adhesion layer. Copper atoms exhibit high mobility in silicon and silicon dioxide, potentially diffusing into these materials and causing device failure or leakages. An aluminum barrier layer prevents this copper diffusion while simultaneously enhancing adhesion between copper and the underlying substrate. The performance of this Al/Cu stack is heavily influenced by deposition parameters including power, pressure, and temperature, which must be optimized to achieve the desired film properties. Post-deposition annealing is employed to reduce stress and improve the microstructure of the metallization system, though temperature limits must be observed to prevent interdiffusion between the layers or degradation of the barrier properties. Both layers were deposited using thermal evaporation for our laboratory.

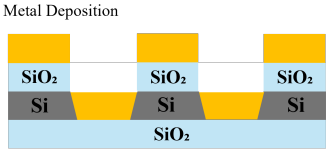


Fig. 8: Metal Deposition over Patterned Substrate

B. Characterization Tools

Microfabrication processes involve multiple stages where precise control over physical dimensions, film properties, and surface morphology is essential. At each stage, whether following oxidation, photolithography, etching, or deposition, characterization plays a critical role in validating the success and uniformity of the process. Key parameters such as layer thickness, etch depth, step height, and surface roughness must be evaluated to ensure fabrication fidelity and yield. A wide array of characterization methods exists, ranging from routine lab tools to highly advanced analytical instruments. Techniques such as stylus profilometry, ellipsometry, and optical microscopy are commonly used for rapid, non-destructive inspection or metrology. More advanced systems, such as scanning electron microscopy (SEM), atomic force microscopy (AFM), or X-ray photoelectron spectroscopy (XPS), offer high-resolution analysis in industrial and research settings but were beyond the scope of this study. In this work, two widely used characterization tools;stylus profilometry and ellipsometry were employed to monitor film thickness and surface topography.

1) Profilometer: A profilometer is an instrument used to measure the surface profile and step height variations on a wafer, providing detailed information about the thickness

of deposited or etched layers. It typically operates using a fine stylus that physically scans across the surface of the sample, detecting vertical displacements as it moves over features. These displacements are converted into a surface profile that reveals the topography of the sample. Profilometry is essential in microfabrication for verifying layer uniformity, measuring trench depths, and ensuring process accuracy during fabrication steps such as etching and deposition.

2) Ellipsometer: Ellipsometry is an optical technique used for measuring the thickness and optical properties of thin films. It works by analyzing the change in polarization of light reflected off the surface of a sample. For this lab, the ellipsometer was used to measure the thickness of the thermally grown silicon dioxide layer on the wafer surface. The system compared measured reflectance data to theoretical models based on known material properties, allowing for precise determination of oxide thickness. This technique is especially valuable for very thin films where mechanical measurement tools like profilometers are less effective.

III. Methodology

The fabrication procedures were executed in a cleanroom environment, following a sequential microfabrication process as outlined in Section II. The process was designed to replicate standard techniques used in semiconductor manufacturing. Characterization tools were employed at various stages to evaluate film thickness and surface features. The procedural details for each fabrication step are presented below.

1) Pre-Lab Safety Instructions: Before entering the cleanroom, all participants completed a mandatory safety training session specific to the microfabrication lab. This included practical guidance on appropriate behavior in case of emergencies, familiarization with lab layout, and hands-on instruction for correctly wearing personal protective equipment such as gloves, goggles, and cleanroom overalls. Additionally, a Chemical Assessment Form was filled out, documenting the specific hazards, handling procedures, and first aid measures for the chemicals used during the lab, including Acetone, 2-Propanol, AZ 400K Developer, AZ® 4562 Photoresist, and Potassium Hydroxide.

2) Samples Overview : Three 4-inch silicon wafers (W1, W2, W3) with <100> orientation and a thickness of 525 ± 25 µm were used in these labs. A silicon dioxide layer was thermally grown on the wafers using dry oxidation in a high-temperature oxidation furnace (1100 °C) with an oxygen supply (3 L/min). The target oxide thickness was 200 nm, as per the process recipe. The three wafers were similar in properties and selected to ensure consistency in subsequent fabrication and measurements. Fig. 9 shows the wafer sample used in this lab before performing any process on it.

Fig. 9: Silicon wafer with thermally grown silicon dioxide layer prior to processing.

3) Primary Measurements with Profilometer: Veeco Dektak 150, a stylus-based profilometer, shown in Fig. 10, was used to measure surface topography, including step height and trench depth. The wafer was mounted on the stage of the profilometer, and its lateral position was adjusted using x-y knobs. The stylus was lowered to make controlled contact with the surface. Measurement parameters such as scanning range (typically 1–2 mm) and sampling density were configured to suit the feature dimensions. Once started, the stylus linearly scanned the targeted part of the surface while the software collected and displayed profile data. Flatness correction was applied as needed. Step heights and thicknesses were extracted from the profile, and measurement data were saved for analysis.

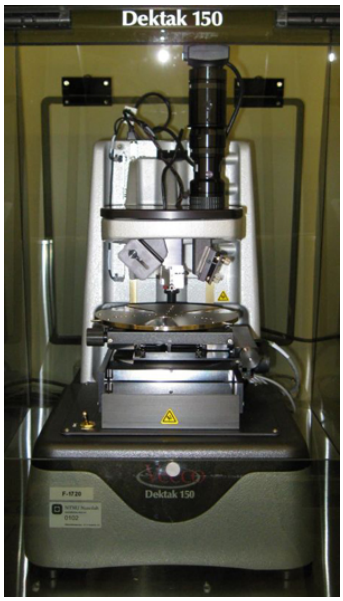


Fig. 10: Veeco Dektak 150 stylus profilometer used for surface topography measurements.

4) Ellipsometer Measurement : A J.A. Woollam alpha-SE ellipsometer shown in Fig. 11 was used to measure thin film thicknesses, specifically for the silicon dioxide layer. Each of the three sample wafers was placed in the device one at a time, with the laser spot aligned to the measurement point. Based on the known optical properties of the material,

an appropriate library model was selected in the software. The system collected reflectance data, fitted it to the selected model, and output the film thicknesses. Measurements were taken and recorded for each wafer for later analysis and comparison.

Fig. 11: J.A. Woollam alpha-SE spectroscopic ellipsometer used for thin film thickness characterization.

5) Cleaning: Prior to photoresist application, each wafer underwent a cleaning procedure to remove surface contaminants and ensure reliable adhesion in the photolithography steps. The wafers were sequentially rinsed with isopropanol and deionized (DI) water to eliminate organic residues, followed by nitrogen gas drying. This cleaning step was carried out immediately before coating to maintain surface quality and process consistency across all three wafers.

6) Photolithographic Patterning: Following substrate cleaning, each silicon wafer was prebaked at $1.50\text{e}2\,^{\circ}\mathrm{C}$ on a hot plate and allowed to cool to room temperature. Photoresist coating was performed using a spin coater equipped with a vacuum chuck to secure the wafers in place. For wafers W1 and W2, approximately $5\,\mathrm{mL}$ of AZ 4562 photoresist (Microchemicals GmbH) was dispensed onto the wafer surface and spin-coated at $3.000\text{e}3\,\mathrm{rpm}$ for $3.0\text{e}1\,\mathrm{s}$, with an acceleration of $1.000\text{e}3\,\mathrm{m\,s^{-2}}$. For wafer W3, a two-step spin coating method was used: $3.500\text{e}3\,\mathrm{rpm}$ for $3.0\text{e}1\,\mathrm{s}$ followed by $4.000\text{e}3\,\mathrm{rpm}$ for an additional $3.0\text{e}1\,\mathrm{s}$, both at the same acceleration.

After spin coating, the wafers underwent a soft bake at $1.15\text{e}2\,^{\circ}\mathrm{C}$ for $3\,\mathrm{min}$ on a hot plate. This step served to evaporate residual solvents from the photoresist layer and improve film stability prior to UV exposure.

The wafers were transferred to a mask aligner system, and the photomask was aligned over the wafer surface. Proximity exposure mode was used to transfer the pattern onto the photoresist using ultraviolet (UV) light. A positive-tone photoresist was utilized, so the exposed areas became soluble during development. Fig. 12 shows the UV exposure system and the photomasks used for pattern transfer onto the wafers.

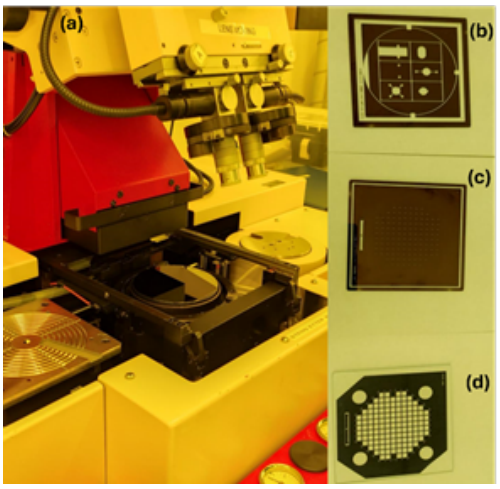


Fig. 12: UV exposure system and photomasks used for pattern transfer onto the wafers.

Fig. 13: (a) Mask aligner equipment, (b)-(d) Different photomask for pattern transfer

The developed wafers were immersed in a tetramethylammonium hydroxide (TMAH) solution to remove the UV-exposed regions of the photoresist. As a positive-tone resist was used, the exposed areas became soluble and were selectively removed, leaving behind a patterned resist layer corresponding to the photomask design. This process is shown in Fig. 14.

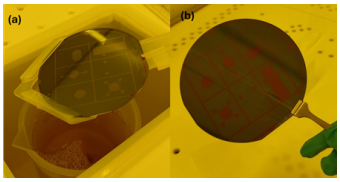


Fig. 14: (a) UV exposed substrate immersed in developer solution (b) clear patterned substrate after undergoing development

Following development, the wafers were subjected to a hard bake at $1.15\text{e}2\,^{\circ}\mathrm{C}$ on a hot plate to stabilize the patterned photoresist. This post-processing step improved the resist's mechanical integrity and adhesion, preparing it for subsequent etching and deposition.

7) Dry Etching via Reactive Ion Etching (RIE): Anisotropic dry etching of the silicon dioxide (SiO_2) layer was carried out using an Inductively Coupled Plasma (ICP) etching system. The process began by placing the wafer on the chuck inside the load lock chamber. After sealing, the chamber pressure was reduced from atmospheric pressure to approximately $1.0\text{e}{-2}\,\mathrm{Torr}$ using a roughing pump. Once the appropriate vacuum level was achieved, the wafer was transferred into the process chamber, which operates at lower pressures in the range of $1.0\text{e}{-3}\,\mathrm{Torr}$ to $1.0\text{e}{-8}\,\mathrm{Torr}$, maintained by a high-vacuum turbo pump.

Prior to plasma ignition, system parameters such as Radio Frequency (RF) power, chamber pressure, and gas flow rates

were configured. A cooling system was used to maintain thermal stability throughout the etch cycle, preventing wafer and photoresist degradation. The etching gasses are a mixture of CHF_3 ($1.70\text{e}1\,\text{sccm}$) and Ar ($3.30\text{e}1\,\text{sccm}$), delivered via mass flow controllers (mfc). This gas mixture leans more towards physical sputtering, giving the process a more anisotropic nature.

Once the gases were stabilized, ICP power was applied to generate plasma, followed by an RF bias applied to the wafer chuck. This combination enabled anisotropic etching through vertical ion bombardment. Upon completion of the etch, the chamber was vented and the wafer was unloaded. Residual photoresist was removed using oxygen plasma ashing to expose the underlying silicon surface in the patterned regions.

8) Wet Etching of Silicon: Following the dry etching step, residual photoresist was removed using oxygen plasma ashing. The wafers were then characterized using a stylus profilometer to assess surface topography and remaining photoresist thickness. To ensure complete removal of residual contaminants, a solvent clean was performed using acetone in an ultrasonic bath, followed by deionized (DI) water rinsing and nitrogen gas drying. Profilometry was repeated post-cleaning to verify surface condition.

Wet etching was carried out using a 10% potassium hydroxide (KOH) solution maintained at 70°C. Two wafers were etched for 23 minutes, and a third was etched for 1 hour 20 minutes to observe time-dependent etch progression. The etching was done in the wet etching station which is shown in Fig. 15. After etching, profilometry was performed to determine the etch depths achieved. Finally, ellipsometry was used to measure the remaining thickness of the SiO_2 layer, providing insight into the etch selectivity and precision.

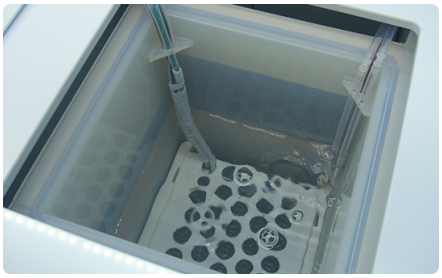


Fig. 15: Wet etching station used for potassium hydroxide (KOH) etching of silicon wafers.

9) Metal Deposition: Metal deposition was performed using thermal evaporation, a physical vapor deposition (PVD) technique. To improve adhesion between copper and the silicon dioxide surface, a thin aluminum film was first deposited as an adhesion and barrier layer.

The wafer was secured onto the dome of the thermal evaporation vacuum chamber which is shown in Fig. 16. Aluminum and copper pellets were loaded into separate crucibles, and the chamber was evacuated to a base pressure in the range of $1.0\text{e}{-5}\,\text{Torr}$ to $1.0\text{e}{-8}\,\text{Torr}$ using a combination of roughing and high-vacuum pumps.

Once vacuum conditions stabilized, aluminum deposition was initiated by resistively heating the aluminum source until evaporation occurred. A Quartz Crystal Microbalance (QCM) sensor was used to monitor and control film thickness in real time. Upon reaching the target thickness, the crucible was sealed to terminate deposition.

Without breaking vacuum, copper deposition followed. The crucible lid was opened, and the copper source was similarly evaporated and deposited onto the wafer surface atop the aluminum layer. The process was again monitored using the QCM until the desired copper thickness was achieved. The chamber was then vented, and the wafer was retrieved for post-deposition analysis.

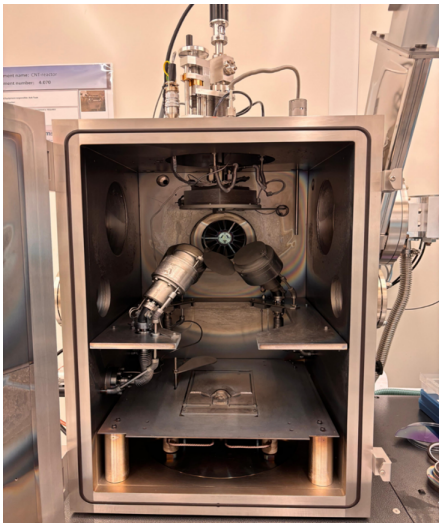


Fig. 16: Thermal evaporation vacuum chamber setup with aluminum and copper crucibles.

IV. Results and Discussions

This section shows the results and discussion:

1) Primary Measurements with Profilometer: As a preliminary step, profilometer measurements were conducted to determine the thickness of various surface layers on the wafers. The measured step heights are summarized in Table I. The tin film exhibited a thickness of approximately 2169.9 nm, as determined from the profilometer trace. The measured thickness of the gold film was approximately 173.16 nm, indicating a very thin deposited layer. Two measurements were taken on separate photoresist-coated regions. Table I shows a photoresist thickness of approximately 1991.64 nm for the

TABLE I: Thicknesses of Different Pre-Processed Wafers

Layer	Thickness (nm)
Tin	2169.9
Gold	173.16
Photoresist 1	1991.64
Photoresist 2	2020.42

first wafer, while the second reports a thickness of around 2020.42 nm, indicating consistent spin coating across wafers. The profilometer measurements showed that the tin and gold layers were deposited with reasonable thicknesses, approximately 2170 nm for tin and 173 nm for gold, indicating that the deposition processes worked as expected. The photoresist layers were also quite consistent, both close to 2000 nm, suggesting that the spin coating was applied evenly. Overall, the results reflect good process control; however, it is worth noting that slight variations could arise due to surface debris or misalignment during measurement. For improved reliability, future work could incorporate an additional verification method to cross-check layer thickness.

2) Ellipsometer Measurement: Ellipsometry was used to validate the thickness of the thermally grown silicon dioxide layer on top of each wafer. As shown in Table II, the measured oxide thicknesses for the three wafers (W1, W2, and W3) were 253.04 $\pm$ 0.02 nm, 234.25 $\pm$ 0.02 nm, and 236.51 $\pm$ 0.02 nm, respectively.

TABLE II: Ellipsometer Measurement Results

Wafer	Measured Thickness (nm)	Tolerance (± nm)
W1	253.04	0.02
W2	234.25	0.02
W3	236.51	0.02

Ellipsometry results showed that the silicon dioxide layers were slightly thicker than the 200 nm target, with measured values ranging between 234 nm and 253 nm across the three wafers. These small variations are likely attributed to differences in heat distribution and gas flow dynamics during the oxidation process. Nevertheless, the values remain within a reasonable and acceptable range. The measurements were consistent and precise, indicating that the thermal oxidation process was well controlled. Additionally, no issues related to coating adhesion were observed, suggesting that the cleaning method using isopropanol and deionized (DI) water was effective. However, future work may explore alternative cleaning solvents, such as acetone, to further evaluate process robustness.

3) Photolithographic Patterning: The design pattern was successfully transferred to the substrate via projection printing to achieve a high-resolution image, thereby defining the pattern for the subsequent etching of the SiO_2 layer. The photoresist layer also served as a mask during the SiO_2 etching process, protecting the regions not intended to be exposed to the developer solution.

To determine the photoresist thickness after soft bake and hard bake, a stylus profilometer (Dektak 150) was used. The thickness values for all three wafers are presented in Table III. A noticeable reduction in thickness was observed for each wafer following post-bake processing. This validates the solvent evaporation effect during baking at elevated temperatures, resulting in thinner and more stable photoresist films. The baking process improves the mechanical integrity and thermal stability of the photoresist, enhancing its performance in subsequent processing steps.

Furthermore, post-bake treatment of the substrate helps solidify the remaining photoresist, thereby improving its durability during later stages. These results underscore the importance of hard baking for removing residual solvents and moisture. This step enhances photoresist adhesion to the substrate and reduces surface roughness—factors that are essential for high-resolution pattern transfer. The hardened resist becomes more resistant to deformation, delamination, or lifting during aggressive processes such as wet etching, plasma etching, ion implantation, or metal deposition.

TABLE III: Thickness of photoresist before and after post-baking process

Condition	Wafer 1 (nm)	Wafer 2 (nm)	Wafer 3 (nm)
Before post-bake	6260.36	6466.27	6412.68
After post-bake	6070.79	6268.27	6312.35

4) Dry Etching: After development, both photoresist (PR) and SiO_2 were present on the wafer surfaces. Dry etching was then performed to selectively remove the exposed SiO_2, with the unexposed PR serving as a masking layer. Through this process, the underlying silicon was exposed, while the protected regions were left intact.

To complete the process, the remaining photoresist was removed using O_2 plasma etching. This step effectively cleaned the wafer surface, leaving behind the desired pattern in silicon and SiO_2. Fig 17 shows the final layer structure at this stage, and Fig 18 illustrates the sequence of steps a wafer undergoes from development to etching, showing how its appearance changes at each stage.

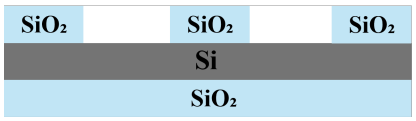
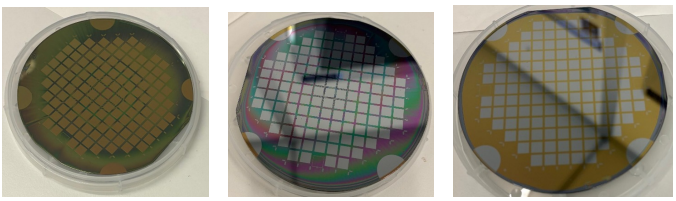


Fig. 17: Final layer structure after PR removal and etching.

Removing the PR is just as important as the etching process itself. Leaving any residual PR on the surface can compromise the quality of the SiO_2 substrate, so it must be thoroughly and properly removed. There are two common pitfalls during PR removal.



(a) after development (b) after dry etching (c) after PR removal

Fig. 18: Wafer at different stages

The first is *incomplete removal*. A thin residual PR layer may remain on top of the silicon, which can interfere with later processing steps. The second is *overexposure to O_2 plasma*, which can oxidize the exposed silicon, forming a thin SiO_2 layer. If the next step involves etching the silicon (e.g., with SF_6), this unintended SiO_2 layer can act as a barrier, slowing down the etch rate and introducing etch delay. It may also act as an insulator, leading to contact resistance during metal deposition.

To avoid such issues, monitoring systems such as endpoint detection, which track the PR layer thickness, can be employed. A quick deoxidation step can also be added to remove any unwanted SiO_2 formed on the silicon surface. In some cases, incomplete PR removal is even visibly detectable to the naked eye.

Therefore, if any residual photoresist remains, the wafer is expected to resemble the structure shown in Figure 18(b). To validate this, the O_2 plasma exposure time was intentionally limited for one of the wafers, allowing some PR to remain. As expected, the resulting wafer was observed to closely match the appearance shown in Figure 18(b), thereby supporting the hypothesis.

An interesting observation was made after the development process. As outlined in the methodology, the top surface layers at this stage were composed of photoresist (PR) and SiO_2. Notably, a radial, colorful reflection pattern was exhibited by the PR, which was an unintended result. This effect was attributed to non-uniformity in the photoresist layer, which can be caused by insufficient protection against white light exposure or suboptimal dry etching conditions. After the dry etching step was performed, the effect became more pronounced, implying that the etching process may have also caused damage or degradation to portions of the PR while targeting the exposed SiO_2.

The presence of varying colors across the wafer surface indicates that the PR thickness is not uniform. The radial symmetry of the pattern is characteristic of the spin-coating process, where centrifugal forces cause slight variations in resist thickness. The color variations are the result of *thin-film interference*: at different thicknesses, constructive and destructive interference of reflected light occurs at different wavelengths, producing the observed rainbow-like effect.

This observation also reinforced the findings obtained from the smaller experiment involving O_2 plasma treatment where the photoresist was not fully removed. It can be implied that residual PR may persist, and the interference pattern was readily detectable with the naked eye. This highlights that thin layers of leftover PR, even if minimal, can be qualitatively assessed through optical inspection due to their characteristic interference effects.

5) Wet Etching of Silicon: To evaluate the progression and selectivity of the wet etching process, thickness measurements were recorded at three key stages: after dry etching, after ultrasonic and acetone-based cleaning, and following wet etching in 10% KOH at 70°C. These values are summarized in Table IV. Wafers 1 and 2 were etched for 23 minutes, while Wafer 3 underwent extended etching for 1 hour and 20 minutes. Profilometer measurements indicated a slight reduction in layer thickness following ultrasonic treatment, confirming partial removal of residual photoresist. Substantial increases in measured depth were observed after wet etching, reflecting significant silicon removal due to the anisotropic etching action of KOH. The much higher thickness value observed for Wafer 3 is attributed to its longer exposure time in the etchant solution.

TABLE IV: Thickness measurements of wafers after sequential processing steps

Wafers	**Thickness Measurements (nm) after**		
	Dry Etching	**Ultrasonic & Acetone Treatment**	**Wet Etching**
Wafer 1	752.63	726.19	18815.79
Wafer 2	655.48	649.25	18744.50
Wafer 3	693.86	660.25	73865.00

The profilometry results after wet etching clearly demonstrate a time-dependent increase in etch depth. Wafers 1 and 2, etched for 23 minutes, both exhibited etch depths of approximately 18.8 µm, aligning well with the expected etch rate of Silicon along with $\langle 100 \rangle$ direction in 10% KOH at 70°C (approximately 46 µm/h) . This confirms the characteristic anisotropic behavior of the etching process, with uniform and predictable material removal.

In contrast, Wafer 3, etched for 1 hour and 20 minutes, showed a significantly deeper etch depth of around 73.9 µm. This increased depth is consistent with the extended etching time and reflects the relatively linear relationship between time and etch progression under constant conditions. The prolonged exposure may have also enhanced verticality and definition of the etched features, though it could result in additional, unintended material removal.

To further analyze the impact of wet etching, ellipsometry was used to measure the thickness of the SiO_2 layer before and after etching. The results, presented in Table V, indicate a reduction in oxide thickness. Although KOH typically shows high selectivity for silicon over that for silicon dioxide, the observed reduction suggests partial etching of the oxide layer during prolonged exposure. This is a relevant consideration in process design when oxide preservation is critical for masking or insulation.

TABLE V: Thickness of SiO_2 layer before and after wet etching

Wafer	**Thickness of SiO_2 Layer (µm)**	
	Before Wet Etching	**After Wet Etching**
Wafer 3	236	141

Fig. 19 shows the appearance of the wafer following wet etching.

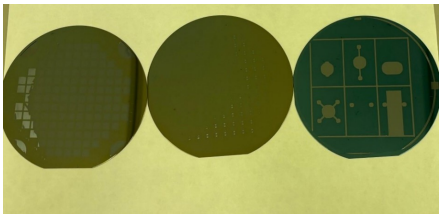


Fig. 19: Post-wet etching appearance of the wafer.

These results demonstrate the sensitivity of the KOH etch process to both time and material interfaces and reinforce the importance of optimizing etch duration to balance material removal with layer protection.

6) Metal Deposition: The thermal evaporation process resulted in the successful deposition of a bilayer metallic film on the wafer substrate. According to measurements recorded by the Quartz Crystal Microbalance (QCM) sensor, the final film thicknesses were 247 nm for the aluminum adhesion layer and 712 nm for the copper layer, as detailed in Table VI. These

TABLE VI: Thermal Evaporation Deposition Results for Al/Cu Bilayer Structure

Layer	Material	Thickness (nm)	Function
Top	Copper	712	Conductive layer
Bottom	Aluminum	247	Adhesion/diffusion barrier

thickness values align with the real-time deposition profiles monitored during the experiment, illustrated in Fig. 20 and 21.

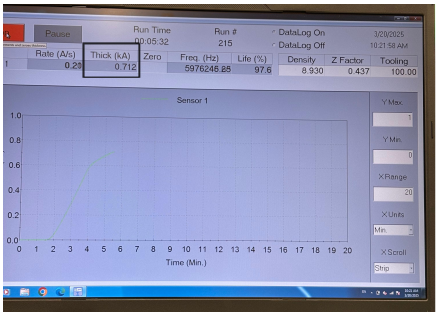


Fig. 20: Copper Thickness

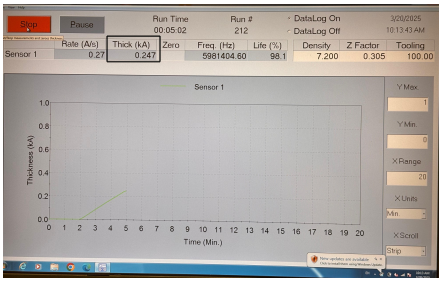


Fig. 21: Aluminum Thickness

Visual inspection of the wafer after deposition revealed a uniform, metallic copper surface with the characteristic reddish-brown color and no visible defects, indicating consistent material coverage across the wafer (Fig. 22). Only clamped edges of the wafer during the deposition show areas without aluminum or copper deposition.

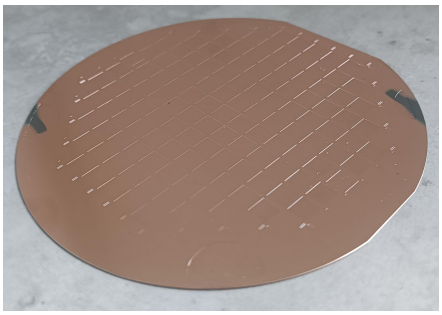


Fig. 22: Wafer after aluminum and copper deposition

The aluminum layer provides sufficient adhesion between the silicon substrate and copper film, while the copper layer offers adequate conductivity for potential electronic applications. The multi-crucible configuration proved particularly advantageous, maintaining vacuum integrity throughout the deposition sequence and preventing oxidation or delamination at the critical aluminum-copper interface. The real-time thickness monitoring by the quartz crystal microbalance sensor enabled precise control over the deposition process for both layers. It is important to note that the sensor readings reflect deposition at the sensor location, which may vary slightly from the wafer due to geometry or shielding effects. The seamless transition between aluminum and copper depositions, achieved by manipulating the crucible lids without breaking vacuum, minimized cross-contamination risks and preserved film purity. This approach represents an efficient methodology for creating multilayer metal structures with well-defined thicknesses, suitable for various microelectronic and MEMS applications. Further characterization of the bilayer structure, including resistivity measurements, adhesion testing, and microstructural analysis, would provide valuable insights into film quality and performance characteristics.

V. Conclusion

The microfabrication of silicon wafers is a highly controlled and sequential process that enables the development of intricate micro and nanoscale features essential for modern semiconductor devices. However, this fabrication on the nanoscale requires intricate processing steps such, wafer cleaning for contaminants removal to ensure optimal surface conditions for subsequent processing. The application of photoresist via spin coating and its subsequent exposure and development through photolithography allow for precise pattern definition on the wafer surface. Following development, wet and dry etching techniques selectively remove underlying material to create microstructures, while the photoresist serves as a protective mask. These etching processes are critical for defining device features with high fidelity and aspect ratio. Finally, metal deposition is carried out to form conductive pathways or

electrodes, completing the functional elements of the device. The importance of each fabrication process step was validated via this work, haven successfully fabricated three different patterned silicon wafers without or negligible defects and impurities. This underscores the robustness of our cleaning, patterning, etching, and metallization process to ensure high-resolution pattern transfer, structural integrity, and device performance. Together, these processes form the backbone of silicon-based microfabrication, supporting a broad range of applications from microelectronics to MEMS devices.

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Process Integration and Micromachining of a Piezoelectric MEMS Microphone Using AlN as a Piezoelectric layer

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***Abstract*—This report presents the fabrication process of a piezoelectric MEMS microphone optimized for bioacoustic sensing, specifically for the detection of elk vocalizations. The device features a circular diaphragm composed of a $1\,\mu m$ thermally grown SiO_2 layer for mechanical support and electrical insulation, a $1\,\mu m$ sputtered AlN piezoelectric layer, and molybdenum and aluminum electrodes, each 200 nm thick, on the bottom and top surfaces, respectively. The ring-shaped top electrode covers approximately 15% of the membrane area near its periphery, enabling efficient charge collection while preserving diaphragm flexibility. The fabrication process begins with high-temperature thermal oxidation, followed by sequential sputtering and patterning of Mo and AlN layers. Via etching is employed to expose the bottom electrode for electrical contact. The top aluminum electrode is then patterned to complete the transduction stack. The microphone structure is released by backside silicon etching to form an acoustic port. The process is fully compatible with CMOS post-processing. Additionally, device parameters such as resonant frequency and sensitivity can be tuned by modifying membrane dimensions and electrode geometry.**

***Index Terms*—MEMS Microphone, Microfabrication, Piezoelectric Aluminum Nitride, Photolithography, etching, Thin-Film Deposition**

I. Introduction

The fabrication of MEMS microphones involves the precise integration of mechanical and electrical structures on a silicon substrate to enable the detection of acoustic signals. In this process, a piezoelectric aluminum nitride (AlN) layer is sandwiched between patterned molybdenum and aluminum electrodes to form a circular unimorph diaphragm. The microphone structure is built layer by layer, starting with thermal oxidation to form an insulating SiO_2 base, followed by sputtering, lithography, and etching to define the electrodes and piezoelectric elements. A key part of the process includes via formation, electrode routing, and deposition of germanium bonding pads for CMOS integration. The final step involves etching a cavity through the backside of the wafer to release the diaphragm and create an acoustic port. This CMOS-compatible process supports scalable manufacturing and enables high-sensitivity, low-power acoustic sensing, particularly for applications such as animal acoustic monitoring.

II. Literature Review

Piezoelectric MEMS microphones have attracted increasing attention due to their inherent ability to convert mechanical pressure into electrical signals, offering advantages such as low power consumption, robust frequency response, and seamless CMOS integration. Recent research in this area spans three critical dimensions: material innovation, structural design, and process integration.

Fabrication typically begins with a silicon or silicon-on-insulator (SOI) wafer. An insulating layer—commonly SiO_2 or Si_3N_4—is formed using thermal oxidation or LPCVD. Bottom electrodes such as Pt, Mo, or Au are deposited by sputtering, followed by the piezoelectric layer, which may be AlN, ScAlN, ZnO, or PZT, applied via sputtering, MOCVD, or sol-gel spin coating. Top electrodes are patterned using photolithography, followed by either lift-off or dry etching. Final device structures, such as membranes or cantilevers, are defined through bulk or surface micromachining, often using wet etching (TMAH, KOH) or DRIE with buried oxide as an etch stop.

Segovia-Fernandez et al. [1] developed a monolithic AlN-based microphone using Al–Ge eutectic bonding, achieving wafer-level CMOS integration. Lu et al. [2] introduced $Sc_{0.2}Al_{0.8}N$ to enhance piezoelectric performance without compromising thermal compatibility. You et al. [3] used single-crystal PZT and rib-reinforced membranes to boost structural stability and sensitivity.

In terms of architecture, Chen et al. [4] demonstrated unimorph cantilevers to enhance signal-to-noise ratio (SNR), while Liu et al. [5] built a resonant ZnO cantilever array optimized for respiratory monitoring. Lu et al. [2] integrated a suspended proof mass to boost low-frequency response via inertial amplification.

Several works also focus on cost-effective processing. Sawane et al. [6] avoided piezo deposition entirely, bonding a prefabricated Ag/PZT/Ag diaphragm with silver epoxy. Ali and Prasad [7] used bulk micromachining and anodic bonding to form a ZnO-based microphone on Pyrex, streamlining both

release and packaging.

Despite these advances, balancing CMOS compatibility, low cost, and high sensitivity remains a significant challenge. Among current trends, monolithic AlN-CMOS integration stands out as a promising route toward scalable, high-performance acoustic sensing systems.

III. Sensor Structure and Operating Principle

This MEMS microphone sensor is based on a circular piezoelectric membrane designed to convert acoustic pressure into electrical signals using a unimorph configuration. The device comprises top and bottom electrodes sandwiching a piezoelectric aluminum nitride (AlN) layer, enabling high sensitivity and compatibility with CMOS post-processing. When acoustic pressure deflects the membrane, the AlN layer undergoes mechanical strain, generating surface charges via the piezoelectric effect. These charges are collected by the surrounding electrodes and routed for signal processing.

Figure 1 Shows a 3D structure of the membrane part which compromises four main functional layers: a passive insulating layer, a piezoelectric layer, and two electrodes. The 3D geometries for the sensor architecture and hierarchical existence of the layers can be further seen in Appendix 1.

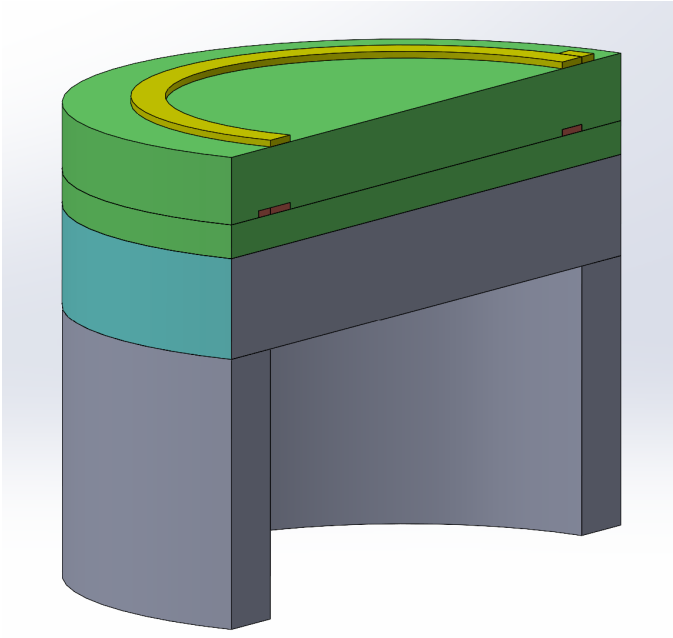

Fig. 1. Illustration of the circular-shaped membrane of the piezoelectric microphone with the outer ring electrodes

At the base is a 1 µm-thick silicon dioxide (SiO_2) layer, which provides mechanical support for the membrane and electrical isolation from the silicon substrate. Above it lies the 1 µm AlN piezoelectric film, selected for its CMOS-compatible deposition, low dielectric loss, and stable piezoelectric coefficients. The top and bottom electrodes, formed from aluminum (Al) and molybdenum (Mo), respectively, are each 200 nm thick and symmetrically positioned on either side of the AlN. The electrode layout follows a ring-shaped pattern near the periphery of the membrane, occupying approximately 15% of its total area to balance sensitivity and structural flexibility. An aluminum via is etched through the AlN to provide vertical electrical contact from the bottom Mo electrode to the top-level interconnect. Signal routing continues to peripheral germanium (Ge) pads situated on patterned SiO_2 standoff structures. These pads serve dual roles: enabling electrical access and facilitating wafer-level eutectic bonding to CMOS circuitry. The complete layer composition and geometry of the MEMS microphone are illustrated in Figure 2, highlighting the material selections optimized for mechanical, electrical, and piezoelectric performance.

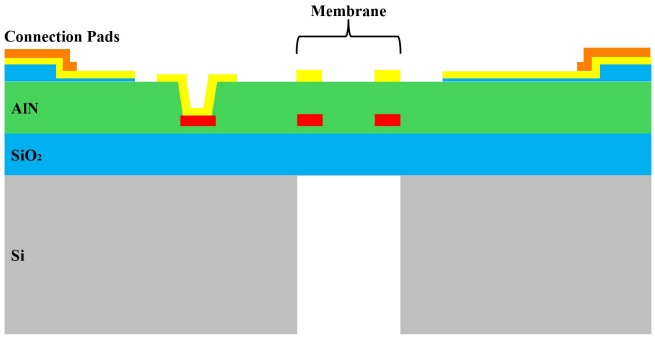

Fig. 2. Cross-section view for the final layers of the fabricated sensor

IV. Fabrication Process

The fabrication is divided into front-end and back-end processes. The front-end encompasses all MEMS sensor structuring—ranging from oxide growth to electrode and diaphragm definition—conducted directly on the silicon wafer. The back-end includes integration with a CMOS wafer using eutectic bonding and subsequent electrical interfacing. The following section outlines the complete front-end process leading up to CMOS-ready bonding structures.

A. Wafer Selection and Pre-Cleaning

A bare, single-side polished silicon wafer with a $\langle 100 \rangle$ crystal orientation and a diameter of 6 inches was selected as the starting substrate. To ensure the removal of organic contaminants, native oxide, and metallic impurities from the wafer surface, a standard RCA cleaning protocol was performed. This included the following sequential steps:

- RCA-1 (SC-1): The wafer was immersed in a solution of NH_4OH:H_2O_2:H_2O (1:1:5) at approximately 75–80 °C for 10 minutes to remove organic residues and particles.
- DI Water Rinse: A thorough rinse in deionized (DI) water was carried out to eliminate chemical residues.
- RCA-2 (SC-2): The wafer was then treated in a solution of HCl:H_2O_2:H_2O (1:1:6) at 75–80 °C for 10 minutes to remove ionic and metallic contaminants.
- Final DI Rinse and Drying: The wafer was rinsed again in DI water and dried using a nitrogen blow or spin dryer.

This cleaning process ensured a pristine silicon surface, free of contaminants, suitable for high-quality thermal oxidation in the subsequent step. Figure 3, shows the clean silicon wafer.

Fig. 3. Unprocessed bare silicon wafer

B. Wet Thermal Growth of SiO_2 Base Layer

Following the RCA cleaning process, the next step involves the formation of a silicon dioxide (SiO_2) base layer on the clean $\langle 100 \rangle$ silicon substrate. This oxide layer serves as both an electrical insulator and a mechanical component of the diaphragm structure in the MEMS microphone. Owing to the absence of any metal or temperature-sensitive layers at this stage, high-temperature processing is permissible, allowing the use of thermal oxidation techniques to achieve a dense, high-quality oxide film.

Wet thermal oxidation was selected for this step due to its significantly faster growth rate compared to dry oxidation and its suitability for forming moderately thick structural oxides. The wafer was placed in a horizontal furnace oxidation system and subjected to a water vapor (H_2O) ambient at 1000 °C. Under these conditions, wet oxidation allows the growth of approximately 6–7 nm of SiO_2 per minute on bare silicon, as documented in standard oxidation models and fabrication literature [1]–[3]. Based on this rate, a target thickness of approximately 400 nm was achieved by maintaining the wafer in steam ambient for approximately 60 minutes. This thickness was chosen to ensure sufficient electrical insulation from the silicon substrate and to provide mechanical support for the subsequent molybdenum and aluminum nitride layers.

The wet oxidation process proceeds according to the Deal–Grove linear-parabolic growth kinetics, which predict rapid initial oxidation followed by a gradual reduction in growth rate as the oxide thickens [4]. For (100)-oriented silicon, empirical studies and fabrication texts confirm that wet oxidation at 1000–1100 °C reliably yields oxide thicknesses in the range of 350–800 nm in one hour, depending on specific furnace calibration and ambient control [1], [3], [5]. Figure 4 shows the thermally grown oxide layer over silicon.

Fig. 4. Thermally grown oxide over silicon substrate

C. AlN Seed Layer Deposition

The fabrication continues with the deposition of a thin AlN seed layer, which defines the crystallographic template for the piezoelectric film. Reactive magnetron sputtering of a high-purity aluminum target in a nitrogen-rich atmosphere is employed, with the substrate held between 300 and 500 °C, the sputtering power adjusted from 1 to 5 kW, and the chamber pressure maintained between 2 and 10 mTorr. Under these conditions, the seed layer grows with its c-axis aligned to match 5° full-width at half-maximum (FWHM) in X-ray diffraction and develops minimal residual stress, both of which are essential for high piezoelectric coupling [8]. This reactive-sputter approach has become the industry standard due to its low cost and seamless integration into CMOS workflows.

Metal–organic chemical vapor deposition using trimethylaluminum (TMA) precursors can yield films with even tighter stoichiometric control and exceptional uniformity, but its added complexity and equipment costs generally relegate it to niche applications [9]. Figure 7 shows the cross section of wafer at this stage.

Fig. 5. AlN seed layer deposited on wafer

D. Molybdenum Electrodes Patterning and Routing

Typical deposition is performed at $2.00\text{e}2\,\mathrm{W}$ to $4.00\text{e}2\,\mathrm{W}$ in an argon plasma at $3\,\mathrm{mTorr}$ to $8\,\mathrm{mTorr}$, producing films $2.00\text{e}2\,\mathrm{nm}$ to $5.00\text{e}2\,\mathrm{nm}$ thick with resistivities of $1.0\text{e}1\,\mu\Omega\,\mathrm{cm}$ to $1.5\text{e}1\,\mu\Omega\,\mathrm{cm}$ and compressive stresses under $5.00\text{e}2\,\mathrm{MPa}$ [10].

Photolithographic patterning defines the electrode geometry: a positive-tone resist is spun, baked, exposed through a mask, and developed to serve as an etch mask. Dry etching by Reactive Ion Etching (RIE) with a Cl_2/BCl_3 gas mixture—operated at 5–15 mTorr and 100–300 W RF power—transfers the pattern into the Mo layer, yielding vertical sidewalls at etch rates of 50–200 nm/min.

Optical emission spectroscopy, tuned to the Mo emission line near 379 nm, provides real-time endpoint detection and prevents over-etching into the AlN [11]. After etching, oxygen plasma ashing and solvent baths remove resist residues, and a brief dip in dilute hydrofluoric acid strips any interfacial oxides, preserving a pristine Mo–AlN interface [12]. Figure 6 shows the deposited Mo electrodes over AlN seed layer.

To relieve thermal-mismatch stress arising from differing thermal expansion coefficients of AlN and Mo, the wafer

undergoes a 400–600 °C anneal in nitrogen, which reduces interfacial strain and enhances adhesion [13].

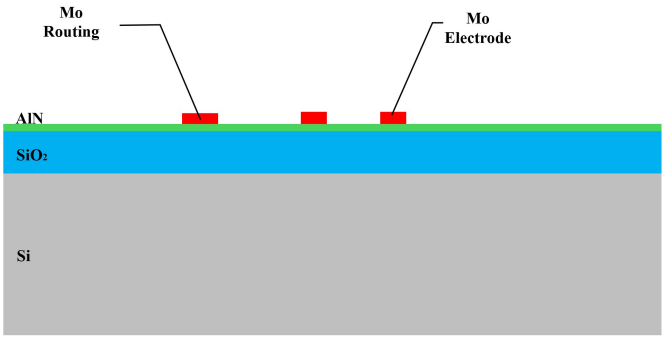

Fig. 6. Mo electrodes and signal routing deposited and patterned on the AlN seed layer

E. Main AlN Piezoelectric Layer Fabrication

Following the preparation of the substrate and seed layer, the main aluminum nitride (AlN) piezoelectric layer is deposited to form the active transduction element of the MEMS microphone. This layer is essential for enabling electromechanical transduction and maintaining membrane integrity.

The AlN layer is deposited using reactive RF magnetron sputtering, a technique well-suited for producing highly c-axis-oriented AlN films [14]. The process uses a pure aluminum target in a controlled atmosphere of argon (Ar) and nitrogen (N_2) gases, with nitrogen content carefully regulated to promote stoichiometric AlN formation, which is crucial for optimal piezoelectric properties and film stability. During deposition, the substrate temperature is typically maintained between 300 and 500 °C to improve crystalline quality while avoiding excessive thermal stress [14], [15].

The final film thickness is approximately 1 µm, selected to meet the acoustic and mechanical requirements of the MEMS diaphragm [16]. Achieving a dominant (002) crystal orientation is critical, as it directly impacts the piezoelectric coefficients and transduction sensitivity. Deposition conditions such as chamber pressure, RF power, and deposition rate are finely tuned to optimize crystal texture and minimize residual stress [14].

After deposition, the AlN film uniformly covers the wafer surface above the SiO_2 layer. This continuous and well-textured film becomes the core of the piezoelectric diaphragm stack as shown in Figure 7

Fig. 7. Cross-sectional view of the MEMS wafer after AlN piezoelectric layer deposition

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F. Formation of Dual-Height SiO_2 Standoff Structures via Sequential PECVD and Lift-Off

To define the mechanical standoff and cavity structures essential for acoustic operation and wafer bonding, a dual-height silicon dioxide (SiO_2) layer was fabricated using a two-step plasma-enhanced chemical vapor deposition (PECVD) and lift-off process as shown in Figure 8. At this point in the fabrication, temperature-sensitive materials such as aluminum nitride (AlN) and molybdenum (Mo) are already present. Therefore, a low-temperature PECVD approach was selected for oxide deposition to ensure compatibility with the underlying layers.

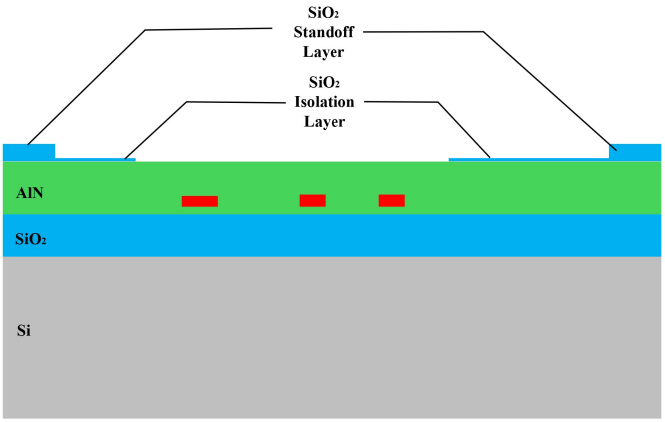

Fig. 8. SiO_2 isolation and standoff layers

In the first sub-step, a positive photoresist layer was spin-coated and patterned via photolithography to define regions corresponding to the lower standoff height. Approximately 1.4 µm of SiO_2 was then deposited by PECVD at a substrate temperature of approximately 300 °C, using SiH_4 and N_2O as precursor gases at a typical pressure of 900 mTorr and RF power of around 20 W. After deposition, lift-off was performed using acetone or an NMP-based solution, resulting in SiO_2 standoffs of the first height in the exposed regions. Subsequently, a second lithography step was used to pattern the photoresist in areas requiring increased standoff height. A second PECVD SiO_2 deposition of approximately 1.1 µm

was carried out under identical process parameters, followed by a second lift-off. This yielded oxide regions with a total height of approximately 2.5 µm, while retaining the original 1.4 µm standoffs in selected areas. This two-step approach ensures dimensional control of cavity height and enables the formation of oxide pedestals that serve as spacers during cap wafer bonding.

This dual-level oxide structuring technique has been validated in prior MEMS literature. Kaul et al. (2022) implemented a comparable strategy for fabricating thermal isolation features in a wake-up receiver MEMS chip using stacked PECVD oxide and photoresist lift-off. Additionally, Prasad et al. (2020) demonstrated reliable lift-off of PECVD-deposited SiO_2 for pattern transfer in MEMS applications, confirming that standard lithographic resist profiles and solvents are compatible with such structuring.

By eliminating high-temperature steps and avoiding depth-controlled etching, this method allows for clean pattern definition and smooth interfaces, which are critical for subsequent wafer bonding and membrane release.

G. Etching of the Aluminum Nitride Layer

After depositing the AlN piezoelectric layer, a via must be opened to allow electrical contact with the buried bottom electrode. This step requires high precision to ensure vertical sidewalls and to avoid damaging the underlying molybdenum (Mo) electrode.

A patterned photoresist mask is first applied to define the via location. The exposed AlN is then etched using Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE), which provides the anisotropic etch profile necessary for clean via formation. Chlorine-based gases such as Cl_2 or BCl_3/Ar are typically used for AlN etching due to their high etch rates and selectivity. Typical process parameters are listed in Table Special care must be taken to stop the etch just before reaching the Mo layer to prevent damaging the electrode, as excessive ion bombardment can affect the conductivity and mechanical properties of the underlying metal [14].

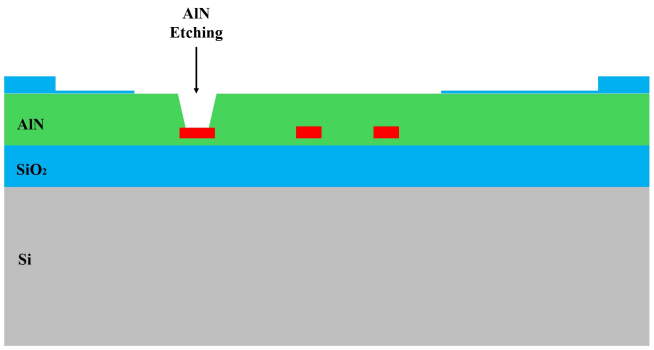

Fig. 9. Cross-sectional view of the MEMS wafer after via etching through the AlN layer

As depicted in Figure 9, a clean, vertical via has been etched through the AlN piezoelectric layer, exposing the underlying Mo bottom electrode. The small vertical cavity represents the via through which an aluminum interconnect will be deposited in the next process step. Special attention is also given to minimizing microtrenching at the via edges, which can arise from highly directional ion bombardment. This is mitigated through careful tuning of gas ratios and chamber pressure [15].

TABLE I
PROCESS PARAMETERS USED DURING DRY ETCHING OF THE ALN PIEZOELECTRIC LAYER TO FORM VIA OPENINGS

Parameter	Value
Plasma Source Power	800 W
Bias Voltage	200 V
Chamber Pressure	5–10 mTorr
Etch Rate	70–80 nm/min

H. Top Aluminum Ring Electrode Fabrication Process

Following via formation, the process advances to the deposition of the second (top) electrode. First, aluminum is deposited using PVD sputtering since it offers great film quality, and control over thickness. Especially for such a thin metal layer. Although it is possible to deposit aluminum directly onto AlN, potential adhesion issues may arise because aluminum exhibits moderate adhesion to AlN surfaces. Thus, a thin titanium layer could improve mechanical stability. After blanket deposition of the Al layer, a new photoresist layer is spin-coated and patterned to define the top aluminum ring electrode, its connection lines and pads, and the electrical paths traversing the vias. An etch-back process is then employed to remove the unwanted aluminum areas, leaving only the desired top electrode structures. Fig. 10 shows the layer structure after this stage. Etch-back is chosen because the surface is no longer flat after stand-off formation, making lift-off unreliable. Finally, the photoresist is stripped after the etching process.

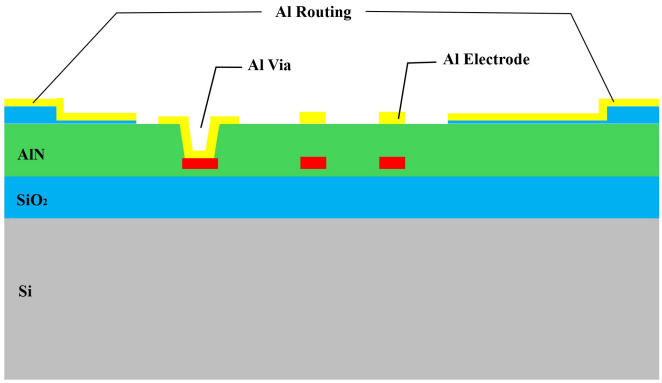

Fig. 10. Cross-sectional view of the MEMS structure after patterning the top aluminum ring electrode

I. Germanium Layer Deposition and Patterning

After defining the bottom electrode and standoff structures, all front-end MEMS fabrication steps are complete. The wafer is now ready for back-end processing via Al–Ge eutectic

bonding with a CMOS carrier wafer.A multi-layer metal stack is deposited sequentially. First, aluminum (Al) is deposited to serve as the top electrode for the microphone membrane. A thin titanium (Ti) layer (approximately 10–20 nm) is then added to act as an adhesion layer between Al and germanium (Ge), as direct adhesion between Ge and Al is poor. Finally, Ge is deposited as the top layer, which will later react with Al during the eutectic bonding step, as illustrated in Figure A3.

The metal stack is deposited using physical vapor deposition (PVD) techniques such as sputtering or evaporation to ensure precise thickness control. The total stack thickness is typically in the range of 0.3–0.5 µm.

Next, a photoresist layer is applied and patterned using photolithography to define bonding pad locations. Ge is selectively etched using either plasma or wet etchants, followed by patterning of the underlying Al/Ti layers to match the Ge pad geometry. This step defines both the eutectic bonding pads and the top electrode routing as shown in Figure 11

Post-patterning cleaning includes photoresist stripping and surface preparation to remove any residues, ensuring clean Ge surfaces suitable for eutectic bonding. A plasma descum (gentle oxygen plasma cleaning) may be employed to remove residual polymers from the Ge surface.

The germanium layer is critical for enabling Al–Ge eutectic bonding between the MEMS wafer and the CMOS wafer. It also forms part of the electrical path connecting the MEMS microphone to the underlying CMOS interface.

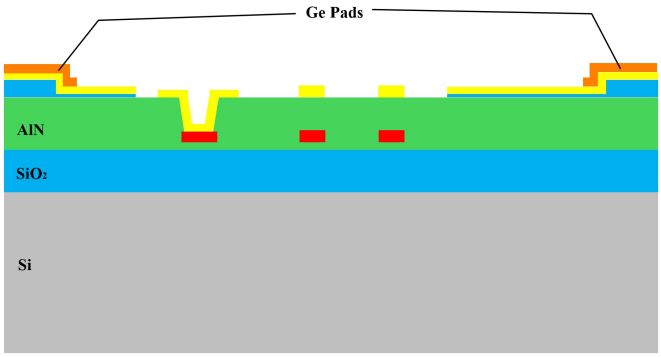

Fig. 11. Schematic of the Al/Ti/Ge metal stack deposited and patterned to form eutectic bonding pads

J. Etched Cavity

Before cavity etching, the backside of the MEMS wafer is patterned with alignment marks. These marks ensure that subsequent through-wafer etches for acoustic ports are properly aligned with the front-side features, including electrodes and the membrane. Although a standoff layer (SiO_2) has been deposited and patterned on the front side to define the bonding gap, no physical cavity yet exists beneath the diaphragm.

To create the acoustic cavity, a Deep Reactive Ion Etching (DRIE) process is performed from the backside of the wafer to etch completely through the silicon. This through-wafer etch exposes the underside of the membrane and forms the open acoustic port beneath the MEMS microphone diaphragm as shown in Figure 12. The DRIE process must be carefully controlled to stop at or near the front-side SiO_2 standoff layer to avoid damaging critical front-side structures.

The etched cavity allows the MEMS diaphragm to vibrate freely in response to sound waves without obstruction from the bulk silicon beneath. It also defines the acoustic volume under the membrane, which directly influences microphone sensitivity [17], [18].

As an alternative or complementary method, the backside cavity can also be formed using wet bulk micromachining. Tetramethylammonium Hydroxide (TMAH) is commonly used for this purpose. TMAH provides anisotropic etching of silicon, and although it is slower and less precise than DRIE, it is considerably more cost-effective [19].

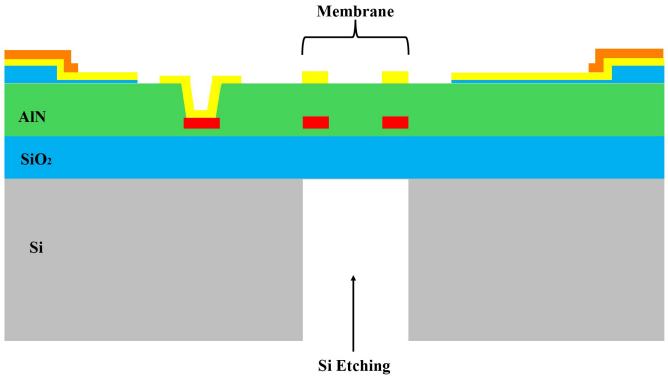

Fig. 12. Cross sectional view of the wafer after etching Si cavity

This marks the completion of the fabrication process; both the front-end and the back-end process; Figure 13 shows the schematic overview of the entire fabrication process. Figure 14 shows the set of the masks that were used for PR process in the process flow shown in Figure 13.

V. Conclusion

In this work, a comprehensive microfabrication process was developed for a piezoelectric MEMS microphone featuring a multilayer unimorph diaphragm structure. The process integrates high-quality wet thermal oxidation for electrical insulation, c-axis-oriented aluminum nitride (AlN) deposition for efficient piezoelectric transduction, and precise molybdenum electrode patterning to define the active sensing region. Dual-height PECVD SiO_2 standoff layers were implemented using a sequential lift-off method to support CMOS wafer-level integration. The top aluminum electrode and Al–Ge eutectic bonding pads were subsequently formed to enable electrical interfacing and back-end packaging.

Finally, a backside cavity was etched using Deep Reactive Ion Etching (DRIE) to release the membrane and define the acoustic port. This CMOS-compatible and scalable fabrication flow provides a robust foundation for high-performance, low-power MEMS microphones in bioacoustic and other sensing applications.

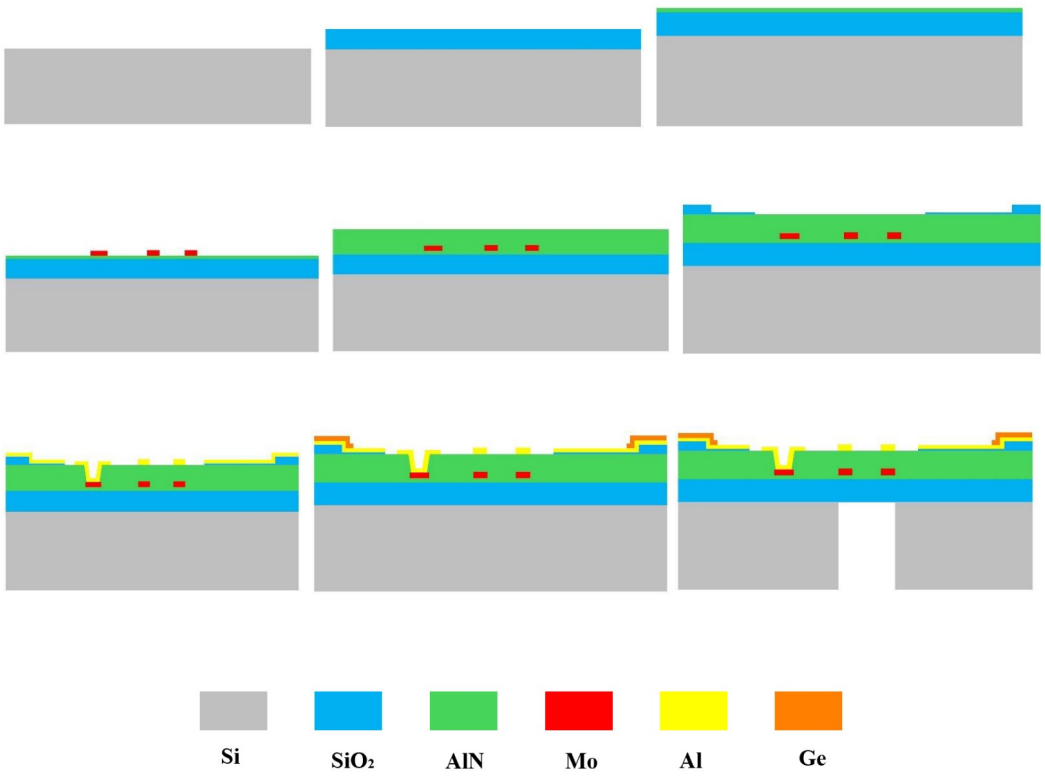

Fig. 13. Schematic overview of the fabrication process for microphone

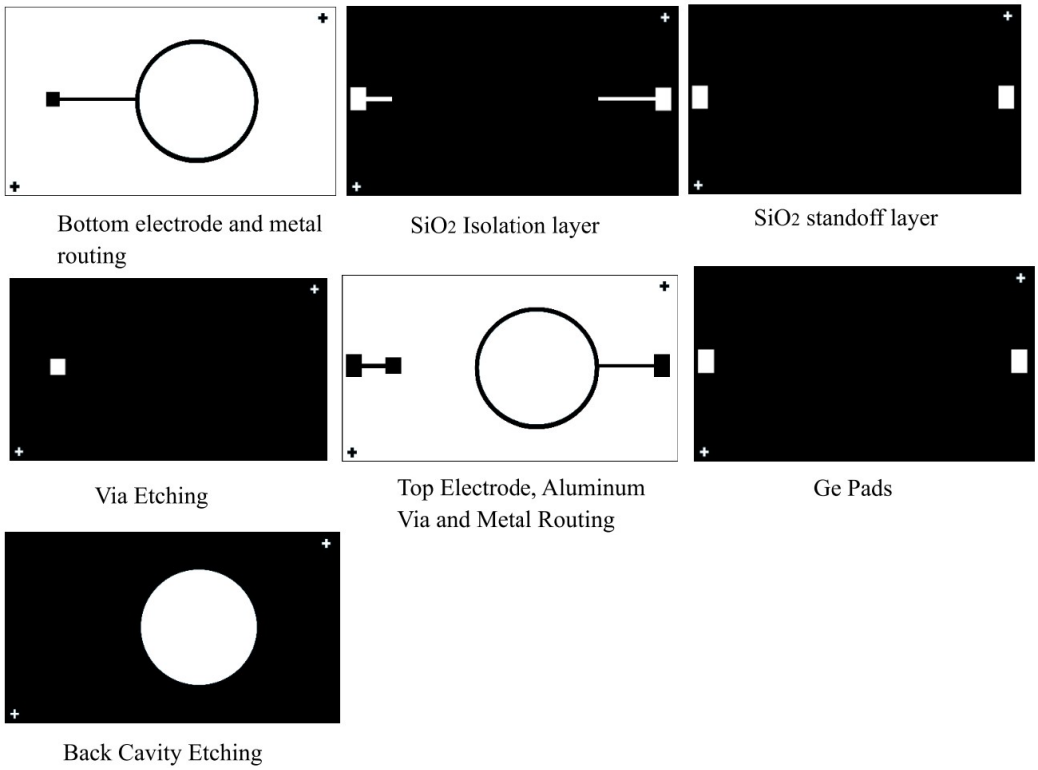

Fig. 14. Overview of the masks used in the Fabrication Process

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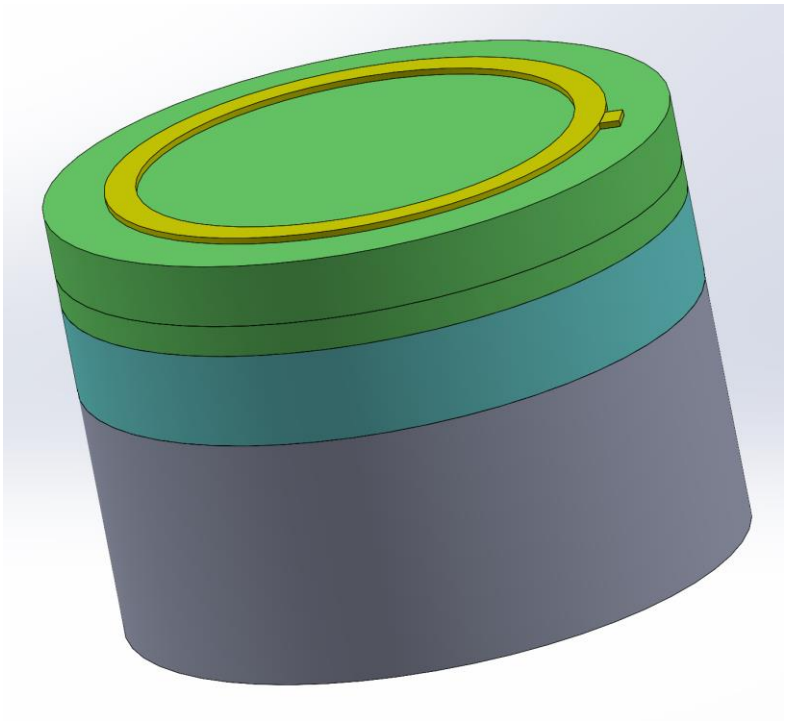
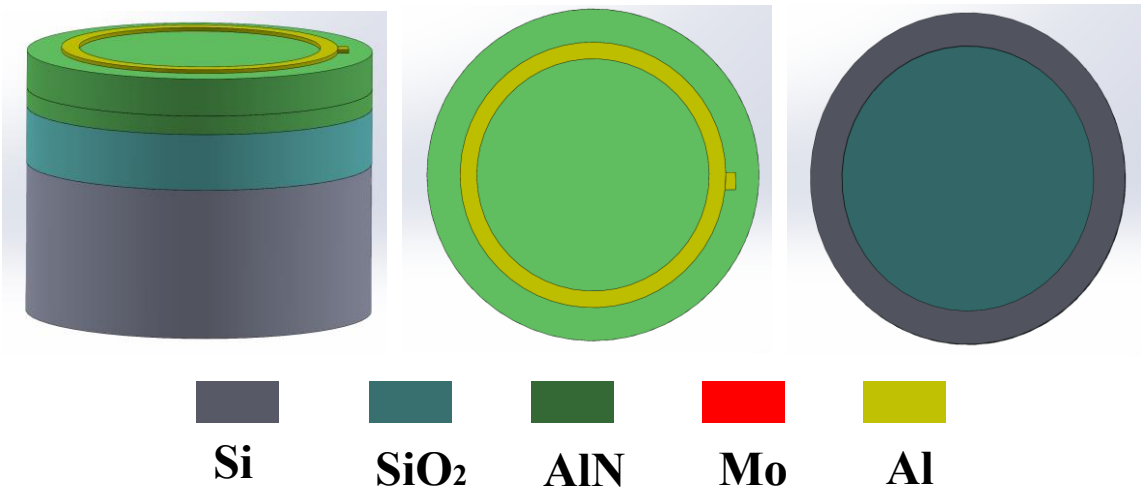
Appendix 1

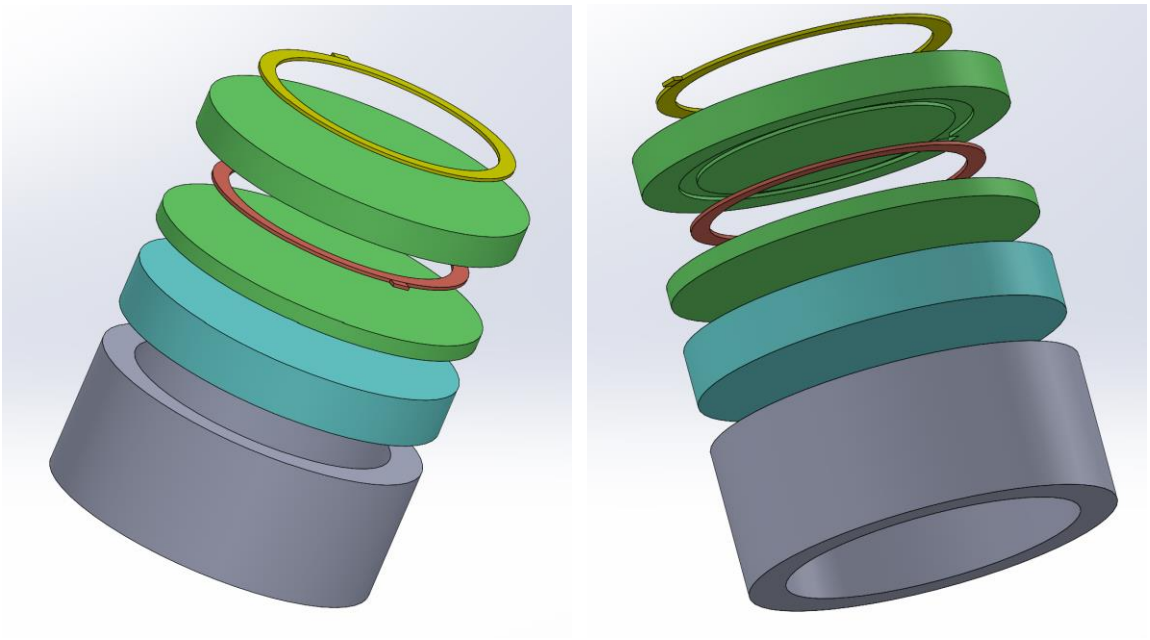
3D Model (Isometric View) of MEMS Microphone with all layers:



Right, Top, Bottom View of Microphone Sensor:



Exploded View of Sensor (showing the hidden Molybdenum Electrodes):



Si SiO_2 AlN Mo Al